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Original Article

A Novel Patterned Ground Shield with Interleaved Metal Dummy for Q-Factor Enhancement in On-Chip Spiral Inductors

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Abstract:
A novel patterned ground shield (PGS) structure for on-chip spiral inductors is proposed to significantly enhance the quality factor (Q-factor) while adhering to advanced process design rules. The structure features an L-shaped interleaved polysilicon and active region layer, grounded through a "米"-shaped Metal-1 grid, coupled with a parallel metal dummy fill pattern distributed across all metal layers (Metal-1 to top ultra-thick metal). This dummy pattern, located in the spaces between inductor turns, minimizes the increase in parasitic capacitance to the substrate compared to conventional or bar-type dummy fills. Electromagnetic (EM) simulations demonstrate that the proposed PGS structure achieves a peak Q-factor (Qmax) **2.5 higher** than an inductor with an ideal shield (violating density rules) and maintains the highest Q-factor up to 8.4 GHz. Furthermore, it induces only a **0.86 GHz** shift in the self-resonant frequency (FSR) compared to the ideal case and has negligible impact on the low-frequency inductance. This work provides an effective shielding solution that balances performance enhancement with design rule compliance for RF integrated circuits.

Index Terms— On-chip inductor, quality factor (Q-factor), patterned ground shield (PGS), parasitic capacitance, design rule checking (DRC), electromagnetic (EM) simulation.

1. Introduction

ON-CHIP spiral inductors are indispensable passive components in CMOS radio-frequency (RF) circuits such as voltage-controlled oscillators (VCOs), low-noise amplifiers (LNAs), and mixers. Their performance, particularly the quality factor (Q-factor), often dictates the overall circuit metrics like phase noise, noise figure, and gain [1], [2]. The primary limitation of the Q-factor in silicon-based inductors is energy loss due to eddy currents induced in the conductive substrate [3].

To mitigate this substrate loss, the patterned ground shield (PGS) technique was introduced [4]. By blocking the electric field lines from penetrating the substrate, PGS structures effectively suppress eddy currents. Over the years, several PGS variants have been developed, including the standard polysilicon PGS [4], the patterned floating shield (PFS) [5], the improved PGS with connected edge bars [6], the horseshoe-shaped PFS [7], the Hilbert-curve PGS [8], and the double-layer floating shield [9]. Each variant offers a trade-off between substrate loss suppression, parasitic capacitance introduction, and impact on inductance.

As CMOS technology scales, stringent metal density design rules are enforced to ensure chemical-mechanical polishing (CMP)

uniformity. Filling empty layout areas with metal dummy patterns becomes mandatory. However, placing these dummies indiscriminately under an inductor, especially directly beneath the coils, can significantly increase the parasitic capacitance to the substrate (Csub), leading to a lower self-resonant frequency (FSR) and degraded high-frequency Q-factor [10]. Therefore, a co-design methodology for the PGS and the mandatory dummy fill is crucial.

This paper proposes a novel, DRC-compliant PGS structure that innovatively integrates the ground shield with a strategically placed metal dummy pattern. The core idea is to shape the dummy fill into lines **parallel to the inductor coils and placed only in the spaces between turns**, thereby minimizing the overlap area and hence the added Csub. This structure is compared against two baselines: an inductor with an ideal shield but no dummies (violating DRC), and an inductor with a conventional bar-type dummy fill. Full-wave EM simulations confirm the superior performance of the proposed structure.

II. Proposed PGS Structure and Design

The proposed PGS structure consists of two key components integrated hierarchically, as shown in the layout top views of Fig. 1 and the enlarged image of the new metal dummy in Fig. 2.

A. Primary Ground Shield Layer:

The foundational shield is formed using an L-shaped interleaved pattern of polysilicon and active region layers. This pattern provides the initial blockage of the electric field. A "米"-shaped Metal-1 grid is overlaid and connected to this polysilicon/active layer through a dense array of contacts (vias). This Metal-1 grid is then connected to the AC ground, ensuring a uniform and low-impedance ground potential across the shield area to prevent potential variation that could cause loss.

B. Metal Dummy Fill Strategy:

To comply with metal density rules, a metal dummy fill pattern is implemented across **all available metal layers**, from Metal-1 (M1) to the top ultra-thick metal (UTM) layer. The innovation lies in the geometry and placement of these dummies:

1. **Geometry:** The dummy fill on each layer consists of metal lines.
2. **Placement:** These lines are placed **parallel to the immediately overlying inductor coil segments**. Crucially, they are positioned **only in the spaces (gaps) between the inductor turns** and in the area outside the outermost turn.
3. **Interconnection:** Dummy fills on vertically adjacent metal layers are connected through corresponding vias, forming a three-dimensional grid. This entire 3D dummy grid is finally connected to the primary Metal-1 ground shield grid, tying it to the AC ground potential.

This design ensures that the dummy metal does not lie directly under the main current-carrying coil traces (minimizing capacitive coupling), while still satisfying area coverage requirements. The parallel alignment further helps in maintaining symmetric parasitic effects.

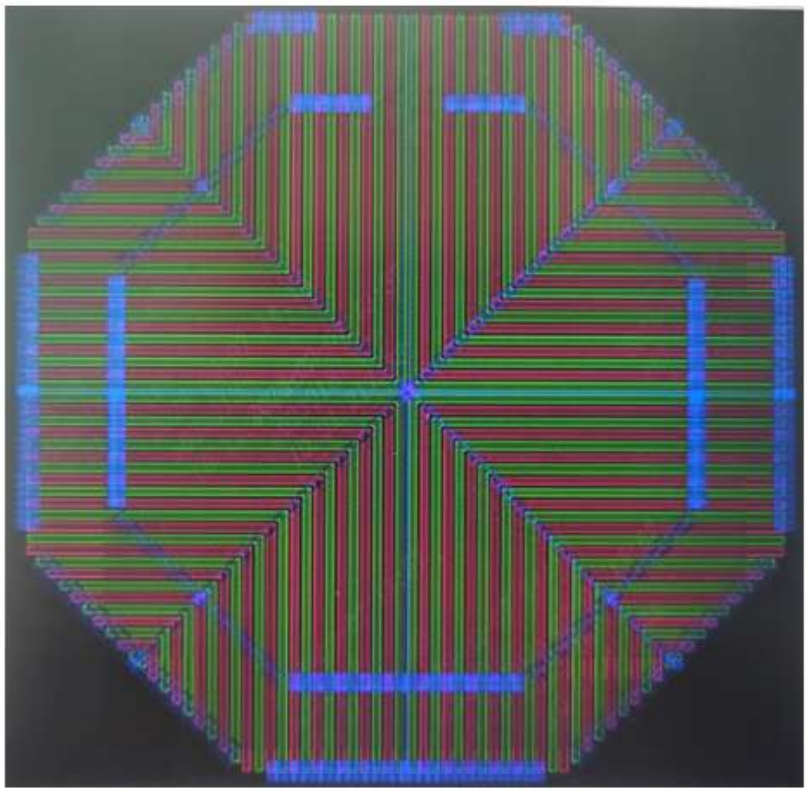
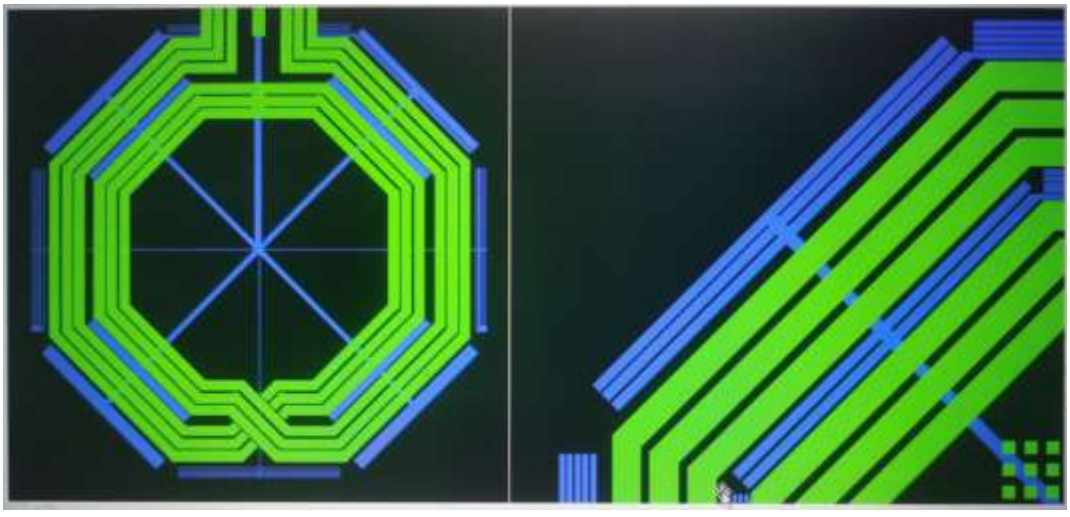


Fig. 1. Top view of the novel PGS illustrating the layered structure of the proposed PGS and dummy fill. The stack shows the silicon substrate, the L-shaped polysilicon/active shield layer, the grounded Metal-1 grid with contacts (CT) connecting to the shield, and the interconnected metal dummy lines from M1 to UTM placed in the inter-turn gap region. The dummy lines on different layers are connected by vias (VIA1-VIAn). The inductor coil resides on the top UTM layer.



(a) (b)

Fig. 2. Layout view of the proposed metal dummy. (a) The complete layout including the spiral inductor (top metal), the "米"-shaped Metal-1 grounding grid. (b) Zoomed-in view highlighting the key innovation: the metal dummy lines (in all layers, represented here collectively) are placed parallel to the inductor coils and confined to the spaces between turns. The dummies are connected to the Metal-1 grid (and thus to ground) via vias (not shown for clarity in this top view).

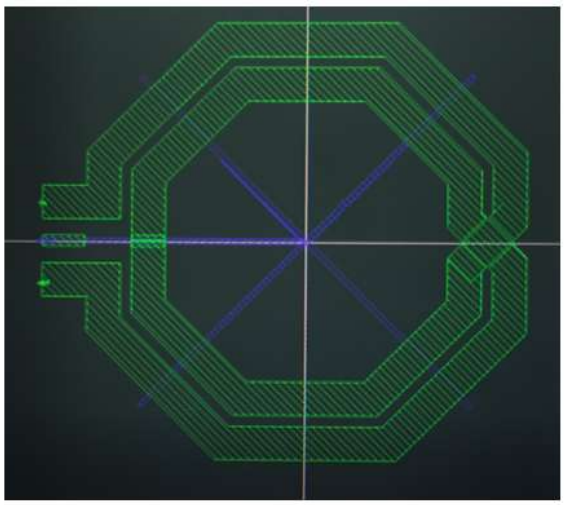
III. Simulation Setup and Comparison Structures

To validate the proposed PGS (hereafter **Inductor 3**), two other inductor structures were designed for comparison on the same 40-nm CMOS process design kit (PDK):

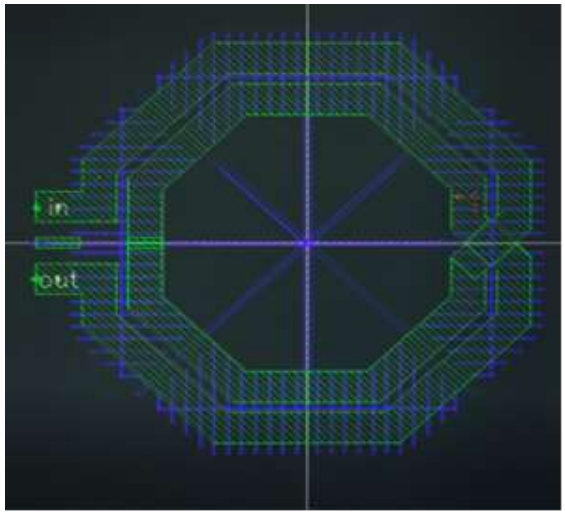
- **Inductor 1 (Baseline - Ideal but DRC-violating):** Features the same primary L-shaped polysilicon/active shield and star-shaped Metal-1 ground grid as the proposed structure. **No metal dummy fill is added** in any metal layers. This represents the ideal performance baseline but violates metal density design rules.
- **Inductor 2 (Conventional Dummy Fill):** Uses the same primary shield as Inductor 1 and 3. A conventional, **perpendicular bar-type metal dummy fill** is placed across all metal layers, typically forming a grid pattern that exists **directly underneath the inductor coils** as well as in the gaps.

All three inductors have identical key geometry parameters: line width (W), line spacing (S), number of turns (N), and inner diameter (ID).

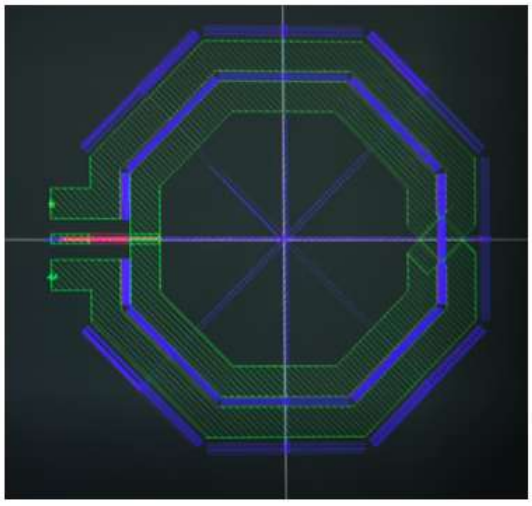
The complete layouts were imported into a 3D full-wave electromagnetic (EM) field solver (ANSYS HFSS). Each inductor was simulated as a three-port network: two ports for the differential inductor terminals (P1, P2) and one port for the shield ground (G). S-parameters were extracted from the simulation. The differential quality factor (Qdiff) and differential inductance (Ldiff) were then calculated using standard formulas [11].



(a)



(b)



(c)

Fig. 3. Layouts of the three inductor structures used for comparison. (a) Inductor 1: Ideal shield (L-shaped poly/active + "米"-shaped M1 ground grid) with NO metal dummy fill (DRC violation). (b) Inductor 2: Same shield as (a) with conventional perpendicular bar-type metal dummy fill placed across all metal layers under the entire inductor area. (c) Inductor 3 (Proposed): Same shield as (a) with the novel parallel, interleaved metal dummy fill placed only in the gaps between turns, across all metal layers.

IV. Results and Discussion

The simulated Qdiffand Ldifff of the three inductors are compared in Fig. 4 and Fig. 5, respectively.

A. Quality Factor (Q-factor) Analysis:

Fig. 4 reveals significant performance differences.

- **Resonant Frequency Shift:** Both Inductor 2 and Inductor 3 show a reduction in FSR compared to Inductor 1, due to the added parasitic capacitance (Cp) from the dummy metal to the substrate. However, the shift for the proposed Inductor 3 (**0.86 GHz**) is substantially smaller than that for Inductor 2. This confirms that placing dummies only in the inter-turn spaces minimizes the Cp increase.
- **Q-factor Performance:** Up to approximately **8.4 GHz**, the proposed **Inductor 3 exhibits the highest Q-factor** among all three structures. Its Qmaxis **2.5 higher** than that of the ideal-but-non-compliant Inductor 1. Inductor 2, with dummies under the coils, shows the most rapid Q-factor degradation and the lowest FSR, as its structure maximizes the Cp.

B. Inductance Analysis:

Fig. 5 shows that the low-frequency (e.g., 1-5 GHz) Ldiff values for all three inductors are nearly identical. This indicates that the proposed dummy fill strategy does not alter the magnetic flux linkage or introduce significant series resistance at low frequencies. The primary impact is on the capacitive parasitics.

C. Discussion:

The superior performance of the proposed structure stems from its **spatial optimization**. By concentrating the mandatory dummy metal in regions of lower electric field intensity (the gaps between turns) and aligning it parallel to the coil, it achieves two goals: 1) it satisfies metal density rules, and 2) it minimizes the degradation of the two most critical inductor figures-of-merit—Q-factor and FSR. The connection of the 3D dummy grid to a robust, low-impedance ground shield also ensures that any coupled currents are safely shunted to ground without creating floating potential nodes that could resonate.

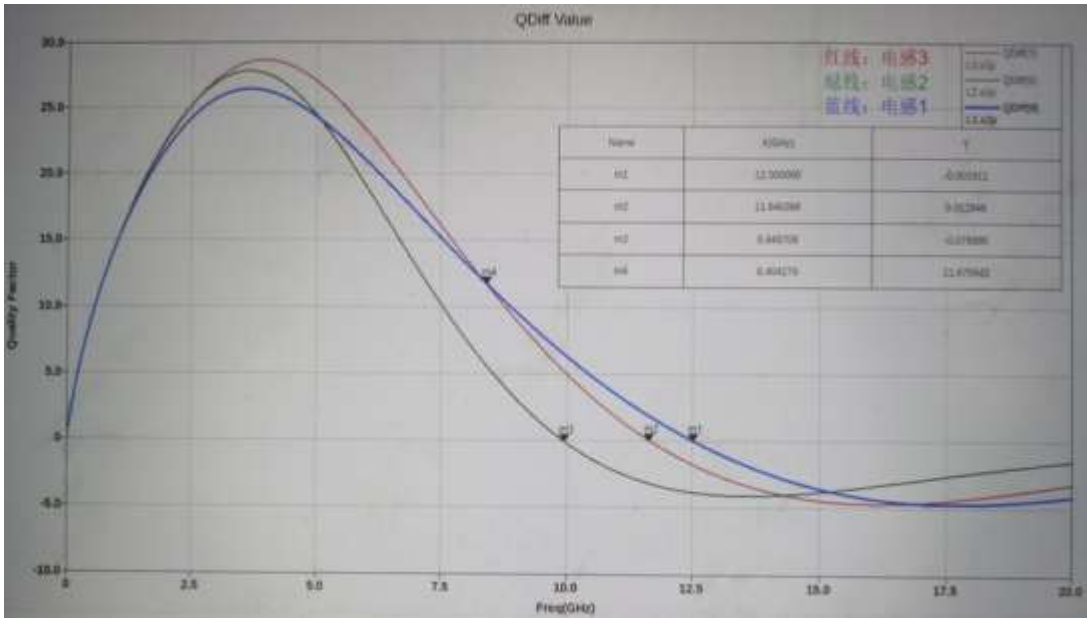


Fig. 4. Simulated differential quality factor (Qdiff) versus frequency for the three inductor structures. Inductor 3 (proposed, blue solid line) shows the highest Q up to 8.4 GHz and a minimal FSR shift (0.86 GHz) compared to the ideal case, Inductor 1 (red dashed line). Inductor 2 (green dotted line) with conventional dummy fill shows severely degraded Q and the lowest SRF.

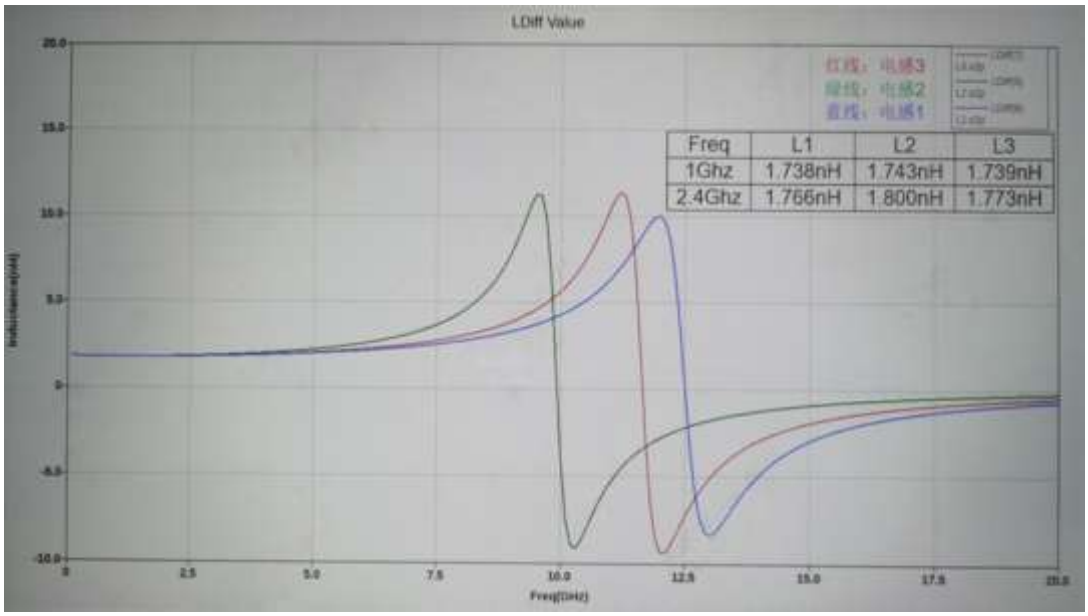


Fig. 5. Simulated differential inductance (Ldiff) versus frequency for the three inductor structures. The low-frequency inductance is virtually unaffected by the different dummy fill strategies. The lines for the three inductors overlap significantly in the low-frequency range.

V. Conclusion

A novel DRC-compliant patterned ground shield structure for on-chip spiral inductors has been proposed and validated through 3D EM simulations. The structure combines a traditional polysilicon/active layer shield with a strategically designed, interleaved metal dummy fill placed only in the spaces between inductor turns and connected across all metal layers. Compared to an inductor with an ideal shield (no dummies), the proposed structure increases the peak Q-factor by 2.5 while causing only a minor SRF shift of 0.86

GHz. Compared to an inductor with a conventional bar-type dummy fill, it demonstrates significantly better high-frequency Q-factor and a higher SRF. This design provides an effective and practical solution for realizing high-Q inductors in advanced CMOS technologies where metal density rules are mandatory, benefiting the performance of critical RF building blocks like VCOs and LNAs.

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